REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-38, 40 and 41 are now in the application. Claims 36-38, 40 and 41 are subject to examination and claims 1-35 have been withdrawn from examination. Claim 36 has been amended and claim 39 has been canceled. No claims have been added.

This after-final Amendment is being filed together with an RCE.

In "Claim Rejections - 35 USC § 112", items 2 and 3 on page 2 of the above-identified Office Action, claim 12 has been rejected as failing to comply with the written description requirement under 35 U.S.C. § 112, first paragraph.

More specifically, the Examiner states that the limitation "wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN" is not described in the Specification and is not enabled by page 20 and Fig. 3 of the instant application. However, it is noted that this limitation was found in original claim 5 of Parent Application No. 10/131,358, which is part of the

original Disclosure and that, as mentioned on page 13, paragraph 4 of the Amendment filed April 7, 2004 in the instant application, embodiment 3, Figs. 8-10 have been elected for prosecution in the instant application, according to the Election of Species requirement made in the parent application and that embodiment 3, Figs. 8-10 is generally described on pages 28-33 of the instant application.

Nevertheless, in order to facilitate prosecution of the instant application, claims 8-10 and 12-14 have been withdrawn in this Amendment, leaving only claims 36-38, 40 and 41 under consideration. Applicants reserve the right to file one or more Divisional applications containing the withdrawn claims at a later date.

In "Claim Rejections - 35 USC § 102", item 5 on pages 3-5 of the Office Action, claims 8-10, 14, 36-38 and 41 have been rejected as being fully anticipated by U.S. Patent No. 6,552,380 to Sato et al. (hereinafter Sato) under 35 U.S.C. § 102(e).

In "Claim Rejections - 35 USC § 103", item 8 on pages 5-6 of the Office Action, claims 12-13 and 39-40 have been rejected as being obvious over Sato in view of U.S. Patent No.

6,335,238 to Hanttangady et al. (hereinafter Hanttangady) under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 36 calls for, *inter alia*, a storage capacitor, comprising:

> a substrate having a trench formed therein, said trench having sidewalls, a bottom, an upper portion and a lower portion;
>
> a collar disposed at said sidewalls in said upper portion of said trench;
>
> a lower capacitor electrode;
>
> a storage dielectric disposed at said sidewalls of said lower portion of said trench, at said bottom of said trench and at said collar in said upper portion of said trench;
>
> an upper capacitor electrode being a conductive layer disposed at said storage dielectric in said lower portion of said trench, said conductive layer being formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN;
>
> a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe

filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric, and said doped layer or said doped filling covering said upper capacitor electrode and being disposed at said storage dielectric at said upper portion of said trench;

said storage dielectric being disposed between said collar and said doped layer or said doped filling in said upper portion of said trench; and

said doped layer or said doped filling being suitably doped to reduce an interfacial stress between said storage dielectric and said conductive layer.

Support for the changes is found in previous claim 39 and in the specification of the instant application.

Thus, claim 36 of the instant application, as amended, now calls for the conductive layer being the upper electrode, the conductive layer being formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN, the storage dielectric being disposed between the collar and the doped layer or the doped filling in the upper portion of the trench, and the doped layer or filling being suitably doped to reduce the interfacial stress between the storage dielectric and the conductive layer.

In the rejection of claims 12, 13, 39 and 40 as being unpatentable over Sato in view of Hanttangady in the Final Office Action, the Examiner has alleged that Sato discloses

all of the limitations of those claims except the specific material of the upper electrode and the specific material of the storage dielectric. The Examiner further alleges that all such materials and their uses are well-known in the art for respectively forming an upper electrode and a storage dielectric. Therefore, according to the Examiner, it would have been obvious to select metal-nitride and metal-oxide as known materials in the device of Sato to respectively form the upper electrode and the storage dielectric, since metal oxide would have high permittivity and metal-nitride would provide a better conductor.

The Sato reference relates to a trench capacitor and a method of manufacturing the same and more specifically to the filling of a trench without causing a void, a crack or clearances. According to the background of the invention of the Sato reference, the filling of a trench by sequentially depositing a thin polycrystalline silicon film on sidewalls, depositing an amorphous silicon film containing impurities on the thin polycrystalline silicon film and subsequently performing a heat treatment to cause the amorphous film to flow to fill the trench, results in voids, cracks or clearances in the trench. In order to overcome the formation of such defects, Sato suggests using a silicon germanium film instead of the amorphous silicon film to fill the trench,

wherein the thin polycrystalline film acts as an appropriate liner film with respect to the silicon germanium film and only the silicon film can be flowed. As a result, the inside of the trench can be buried easily without causing a void, a crack or clearance (see column 6, line 65 to column 7, line 4). According to the Sato reference, the silicon germanium film acts as a node electrode (see column 5, lines 59 to 61).

The Hanttangady reference relates to a trench capacitor for use in a DRAM. The trench capacitor includes an outer electrode formed in a substrate, a silicon carbide layer lining sidewalls of a trench, a high permittivity storage dielectric covering the silicon carbide layer and an inner electrode of a metal such as titanium nitride or a tungsten-based conductor covering the silicon carbide layer and filling the trench.

Amended claim 36, which reads on embodiment 3 and Figs. 8-10 as mentioned above and in previous correspondence, calls for:

> the conductive layer being the upper electrode;
>
> the conductive layer being formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN (which was previously recited in claim 39);
>
> the storage dielectric being disposed between the collar and the doped layer or the doped filling in the upper portion of the trench; and

the doped layer or filling being suitably doped to reduce the interfacial stress between the storage dielectric and the conductive layer.

The storage capacitor according to amended claim 36 differs from the storage capacitor according to Sato by the fact that the conductive layer of the upper electrode is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN, whereas according to Sato a liner layer of polysilicon is formed between the dielectric and the doped silicon germanium filling.

Furthermore, the storage capacitor according to amended claim 36 differs from the storage capacitor according to Sato by the fact that in the upper part of the trench, the storage dielectric is disposed between the collar and the doped layer or the doped filling, whereas according to Sato in the upper portion of the trench the storage dielectric is disposed between the collar and the polysilicon layer.

Therefore the storage capacitor according to amended claim 36 is novel.

According to the Final Office Action, Hanttangady discloses that the materials of the conductive layer are well known in

the art for forming the upper electrode. Therefore, according to the Examiner, it would have been obvious to use such materials in the device of Sato to form the upper electrode because it would provide a better conductor. The Sato reference and the Hanttangady may both relate to a storage capacitor. However, neither the Sato reference nor the Hanttangady reference relate to the interfacial stress that occurs between a dielectric layer and an upper electrode formed of one of those materials.

In contrast, the present invention relates to stress-reduced layer systems. According to the paragraph bridging pages 1 and 2 of the Specification of the instant application, in layer systems without stress reduction, the problem usually occurs that due to the different lattice constants and the different coefficients of thermal expansion of the materials both at the interface and in the bulk, considerable stresses are generated, which may cause a layer which is applied to become detached from the other layer or stress defects to be produced in the material located below the applied layer.

According to page 10, first full paragraph of the Specification of the instant application, the present invention is substantially based on the discovery that, as a result of the controlled introduction of impurities into a

semiconductor layer, mechanical stresses at an interface between conducting and insulating layers can be reduced, wherein the impurities have to be selected in such a manner that the mechanical properties are modified in a suitable way, while the electrical properties are retained in such a manner that a fully functional electrical component remains possible.

According to the present invention, the interfacial stress which occurs between an insulating layer and a conducting layer is reduced by means of a suitably doped [SiGe] layer which is applied to the conductive layer (see page 28, last full paragraph of the Specification of the instant application). Accordingly, in the storage capacitor according to the present invention, the doped layer is suitably doped to effect a reduced interfacial stress between the storage dielectric and the upper electrode. It is only a suitable combination of the materials of the storage dielectric, the upper electrode and the doped layer with suitable dopants and a suitable doping level which makes it possible to use an upper electrode formed of one of the materials as stated above, because otherwise mechanical stress between the interface of the storage dielectric and the upper electrode would occur.

This is completely different from merely replacing the polysilicon liner layer of the Sato reference with an upper electrode formed of a material known from the Hanttangady reference. For example, according to the Sato reference, Boron is preferably used as a dopant for the silicon germanium film, whereas according to the Specification of the instant application on page 30, third paragraph, arsenic is used as a dopant for the silicon germanium film. Accordingly, the subject matter of the present invention is neither suggested by the Sato reference, the Hanttangady reference nor a combination thereof.

Furthermore, according to Sato, the process of fabricating the semiconductor device includes the deposition of a polycrystalline silicon as a liner film on the entire surface of the trench, the deposition of a silicon germanium film on the polycrystalline film and flowing the silicon germanium film to fill the trench by performing a heat treatment on the silicon germanium film. According to column 6, line 65 to column 7, line 4, the polysilicon film membrane acts as an appropriate liner film with respect to the silicon germanium film and only the silicon germanium film can be flowed during the heating step. There is no indication that the silicon germanium film may be flowed according to Sato with a dielectric layer disposed at the upper portion of the trench

at the collar, as required by claim 36 of the instant application.

Although it is believed that claim 36 is patentable over the prior art as discussed above, it is also noted that claim 41 calls for the doped layer having a dopant distribution with a gradient. As is stated in the last paragraph on page 12 of the Specification of the instant application, a spatially varying doping profile ensures that it is possible both to adapt the stresses at the interface and to reduce the stresses in the bulk.

With regard to claim 41, the Examiner states that the Sato reference discloses that the dopant distribution with a gradient for the silicon germanium layer is selected from the group consisting of B and P. However, corresponding Fig. 4 does not show a dopant gradient in a single layer, but instead shows the dependency of the film resistivity for different samples having different germanium mole fractions and different dopants. Accordingly, a doped layer having a dopant distribution with a gradient is not suggested by the Sato reference.

Accordingly, it is believed that the subject matter of claim 41 is patentable over Sato in view of Hattangady independently of claim 36.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 36 and 41. Claims 36 and 41 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 36.

In view of the foregoing, reconsideration and allowance of claims 36-38, 40 and 41, are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

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Amdt. dated 8/17/06
Reply to Office action of 5/17/06

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

Respectfully submitted,

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